Heavy Ion SEE Test Report for the Micron 4Gbit NAND Flash Memory for MMS

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I. Introduction

This study was undertaken to determine and compare the susceptibilities of 4 Gbit NAND Flash memories from Micron to destructive and nondestructive single-event effects (SEE) for the NASA MMS mission. The devices were monitored for SEUs, errors from individual cells, for SEFIs, errors arising in the control logic, and for destructive events, including latchup, induced by exposing them to a heavy ion beam at the Texas A&M University Cyclotron.

II. Devices Tested

We tested a total of four Micron parts, out of eight available (part number MT29F4G08AAAWP, Lot Date Code (LDC) 744). The parts have 512Mx8 organization with large blocks. That is, the blocks are 128Kx8, with 64 pages/block. Each page is nominally 2Kx8, but they also have 64 redundant columns, which makes the total page size 2112x8. NAND flash normally has some bad blocks which can be screened off. The specification is that no more than 80 of the 4096 blocks will be bad. In our experience, the parts almost always have a few bad blocks, but it is usually a single digit number. Note that with commercial devices, the same lot date code is no guarantee that the devices are from the same wafer diffusion lot or even from the same fabrication facility.

The device technology is 63 nm minimum feature size CMOS NAND Flash memory. All the parts are single die, SLC (single level cells). The chips came in a 48-pin TSOP package, but the plastic had been dissolved on the topside to expose the chips, allowing the beam to reach the chip surface.

Fig. 1. Photo of die

III. Test Facilities

Facility: Texas A&M University Cyclotron
Flux: (5 x 10^3 to 1. x 10^5 particles/cm^2/s).
Fluence: All tests were run to 1E3 to 1E8 p/cm^2, or until destructive or functional events occurred.

Table I: Ions/Energies and LET for this test

TAMU Ions	Energy/ AMU	Energy (MeV)	Approx. LET on die (MeV•cm^2/mg)	Angle	Effective LET
Ne	15	300	2.7	0	2.8
Ar	15	600	8.4	0,45	8.4, 11.8
Kr	15	1260	30.1	0	29.3
Xe	15	1965	54.8	0	53.9

IV. Test Conditions

Test Temperature: Room Temperature for SEU, 70° C for SEL
Operating Frequency: (0-40 MHz).
Power Supply Voltage: (3.3V for SEU, 3.6V (3.3+10%) for SEL). Standard test methods for SEU testing (e.g., ASTM 1192) call for testing at nominal voltage less 10%, because SEU in standard volatile memories is caused by voltages being pulled down. However, flash memories are designed to retain information even at zero volts, so the upset mechanisms are clearly different, here. In addition, we are also looking for control logic errors, which are thought to be due to things turning on when they are not supposed to be on. Reduced voltage would cause an underestimate of the rate for these events. Therefore, we used nominal voltage, 3.3 V, in all tests except latchup tests, which were done at 3.6 V, and also at elevated temperature.

V. Test Methods

Because Flash technology uses different voltages and circuitry depending on the operation being performed, testing was performed for a variety of test patterns and bias and operating conditions.

Test patterns included all 0's, all 1's, checkerboard and inverse checkerboard. In general, all zeroes is the worst-case condition for single bit errors. For a zero, the floating gate is fully charged with electrons. An ion can have the effect of introducing positive charge, which may be enough to cause a zero-to-one error. However, a checkerboard pattern (AA) was used in most of the testing because errors in the control circuitry can cause errors of both polarities. One-to-zero errors are an indication that the errors are coming from the control circuits. Between exposures, all patterns can used to exercise the DUT, to verify that it was still fully functional. However, all patterns are not used on every shot, just because it is time consuming to do so. The maximum clock frequency for these devices was 40 MHz, which is also the frequency used in the dynamic testing.

Bias and operating conditions included:

1) Static/Unbiased irradiation, in which a pattern was written and verified, and then bias was removed from the part and the part was irradiated. Once the irradiation reached the desired fluence, it was stopped, bias was restored, and the memory contents were read and errors tallied.

2) Static irradiation, which was similar to unbiased irradiation, except that bias was maintained throughout irradiation of the part.

Note that these conditions provide no opportunity to monitor functional or hard failures that may occur during the irradiation.

3) Dynamic Read, in which a pattern was written to memory and verified, then subsequently read continuously during irradiation. This condition allows determination of functional, configuration and hard errors, as well as bit errors. In this mode, the number of static bit errors is determined by reading the memory again, after the beam is turned off.

4) Dynamic Read/Write, which was similar to the Dynamic Read, except that a write operation is performed on each word found to be in error during the previous Read.

5) Dynamic Read/Erase/Write, which again was similar to the Dynamic Read and Read/Write, except that a word in error was first erased and then rewritten. In this mode, the words that are read are compared to an "expected" pattern, which is actually the complement of the stored pattern. For this reason, every word is erased, as if it were in error. Because the Erase and Write operations use the charge pump, it is expected that the Flash could be more vulnerable to destructive conditions during these operations.

6) Latchup testing was conducted at 70° C, and 3.6 V, on parts from all three manufacturers. It was expected that high voltage, dynamic test modes would be most likely to result in latchup, so these were emphasized in the latchup testing, but all test modes were checked at least briefly.

7) In this set of experiments, we have included an initial attempt to look at angular effects, which may include multiple bits grazed by the same ion, and other effects due to charge sharing by multiple nodes in the control logic. This test was done with at 45 degrees, but only on two exposures. The rate of destructive effects seemed to be very high on these exposures, so we took a complete set of data at normal incidence first. Unfortunately, we ran out of beam time before we could complete the angular study. But the results suggest that this study has to be completed before these parts are used in space.

The Block diagram for control of the DUT is shown in Figure 2. The FPGA based controller interfaces to the FLASH daughter card and to a laptop, allowing control of the FPGA and uploading of new FPGA configurations and instructions for control of the DUT. Power for the flash is supplied by means of a computer-controlled power supply. The National Instruments Labview interface monitors the power supply for over-current conditions and shuts down power to the DUT if such conditions are detected.

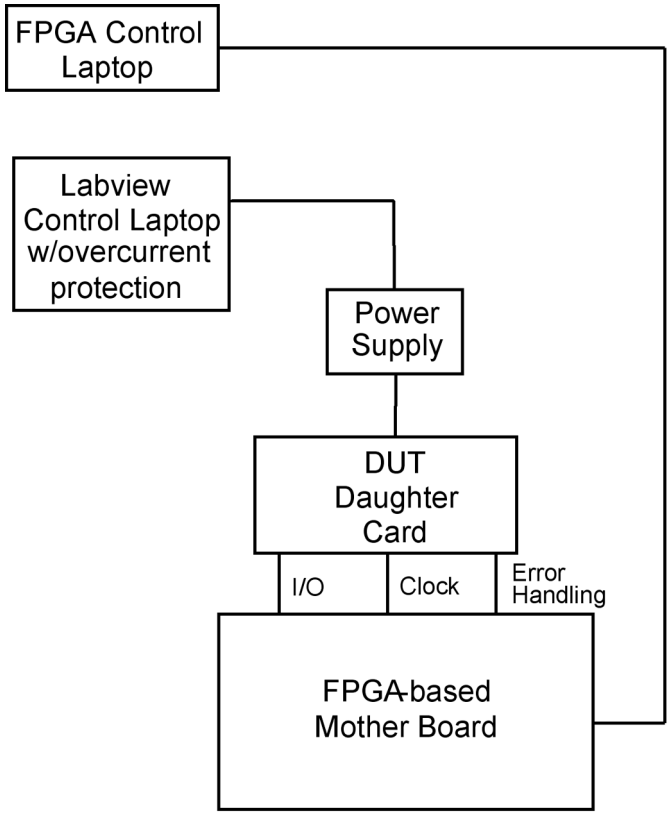

Figure 2. Overall Block Diagram for the testing of the NAND Flash.

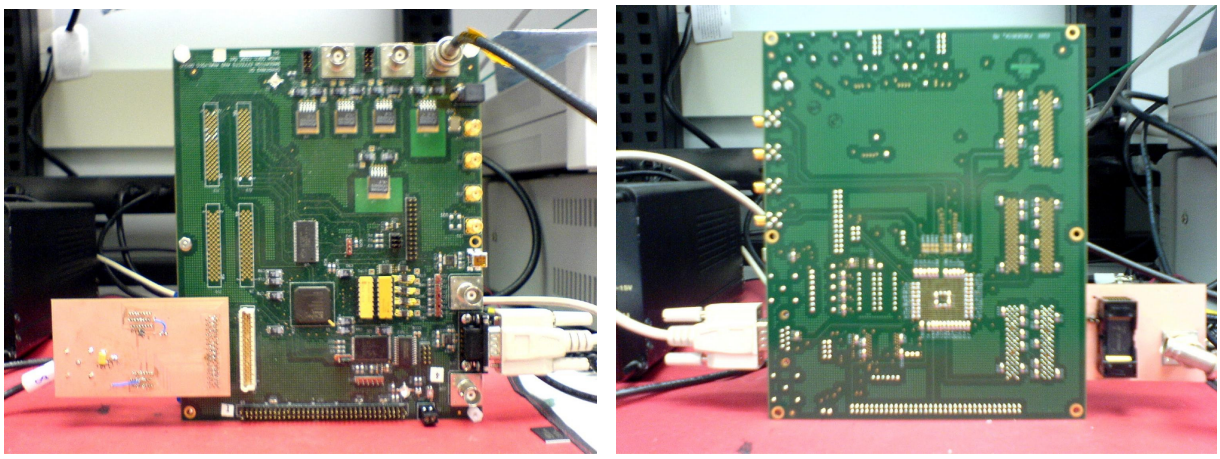

Fig. 3. Front and back views of motherboard and daughterboard, with DUT.

VI. Results

During testing, the DUTs were irradiated with the ions indicated in Table I. The DUT was oriented normal to the incident beam, except as noted. The errors observed in static SEU testing are shown in Fig. 4a, with no bias applied. In Fig. 4a, the vertical axis is in units of cm^2/bit, as is commonly done for SEU testing. The same data is shown in Fig. 4b, with the vertical axis in units of cm^2/device, so that SEFI results can be plotted on the same scale.

Even for the static unbiased case, bit errors and two SEFIs with one destructive failure were observed. The most common SEFI mode, generally, was a Block error. One of the static unbiased SEFIs was a block error, where an entire block was lost, presumably from the effects of a single ion. It is likely that Page/Block errors arise due to upsets in configuration registers in the memory array. The other SEFI was different, affecting some bits in every block in the memory. The destructive failure was the loss of the erase function, probably due to damage to the charge pump, which was surprising only because the charge pump was unbiased. The exposures that produced the SEFIs and the destructive failure were at 45 degrees, because we were trying to determine the worst case angle and the angular dependence of the effects. (In Fig 4b, the angular shots are plotted at LET=11.4, nominal LET/cos θ.) However, we did not have enough parts to do most of the testing under conditions that would cause catastrophic failure. Therefore, we decided to concentrate on getting normal incidence data first, since there had not been any catastrophic failures on several normal incidence exposures. We intended to return to the angular dependence later, but ran out of beam time before that could be completed. We believe the probability of errors in the control circuits is increased at high angles because more charge is generated close to the surface and over a wider area, and, therefore, closer to multiple active device regions. That is, charge sharing between multiple sensitive nodes is increased, compared to an exposure at normal incidence. Because the DUT was not actively exercised during the static exposures, we could not determine exactly when a page/block error occurred, so cross sections are approximate for these error modes.

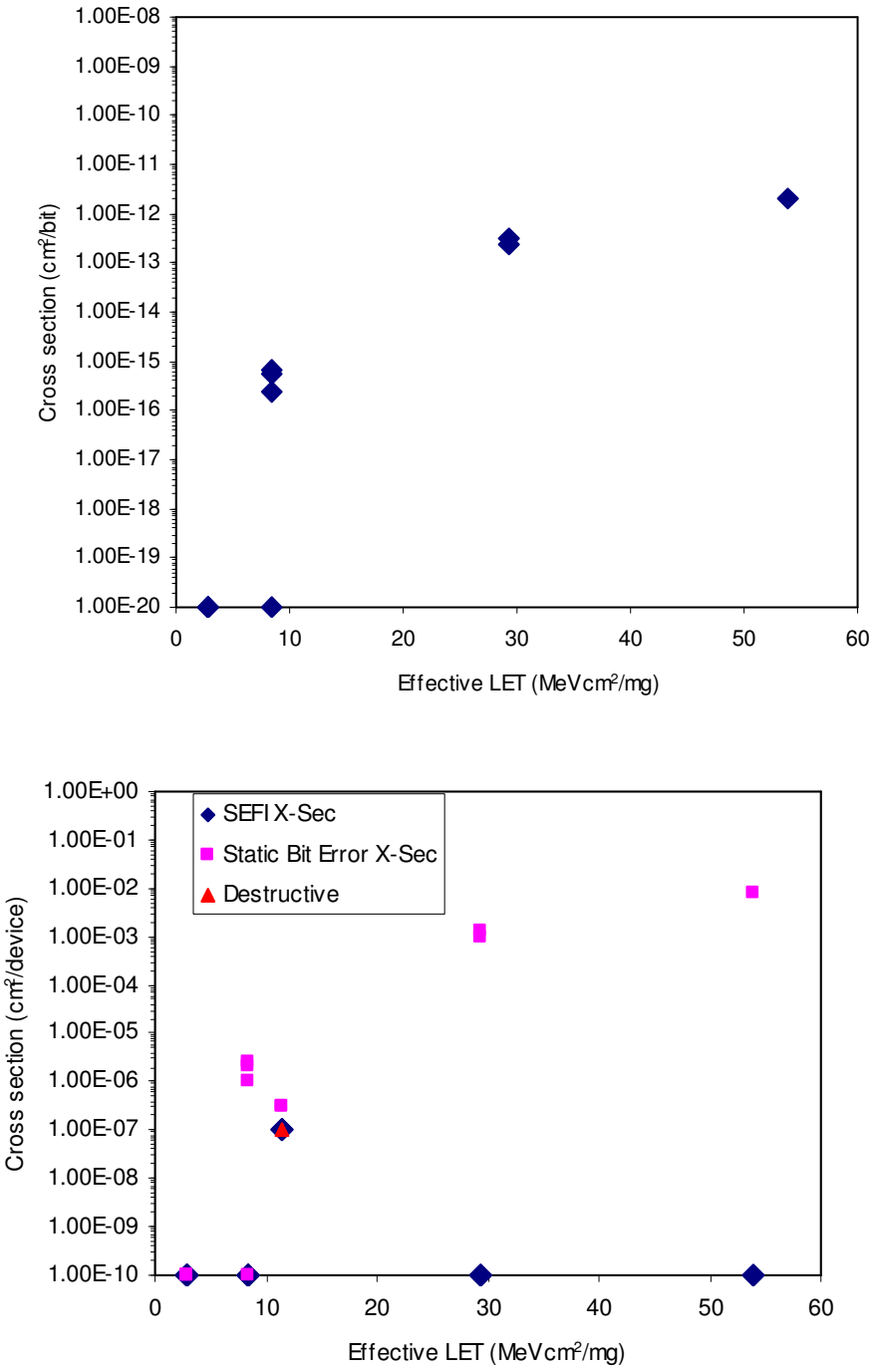

Fig. 4. Results in static test mode: (a) SEU results; (b) SEU results and SEFI results on the same scale.

Here and in the following discussion, bit errors are taken to be single bits, which are flipped, as a result of the interaction with incident ions, normally from zero to one. We do not have the physical to logical address mapping, which would allow us to look for multiple bit errors (error clusters) for these parts. However, in the overwhelming majority of cases of bit errors, there is only one error in a page, or one error in an entire block, which makes it extremely unlikely that there will be multiple bit cells upset from a single ion. This result is consistent with previously

published results on the upset mechanism in flash memory—an ion passing through a floating gate creates a dense charge column, which creates a conducting path between the gate and substrate, which allows charge to leak off the floating gate. Since the ion only hits one gate at normal incidence, only one bit is affected. This situation is far different from that in volatile memories, where charge generated in the Si substrate can be shared across multiple nodes. The only apparent multiple bit errors are due to errors in the control logic, for example, cases where an entire page or a block (or a large part of one) upsets simultaneously. These page and block errors are attributed to errors in the control logic, rather than to the individual bit cells. These are counted as SEFIs (Single Event Functional Interrupt). In general, a SEFI is any event where the entire DUT, or a large part of it, stops working, presumably from an interaction with a single ion. As a practical matter, most of the SEFIs recorded here are block errors, although some involve multiple pages or multiple blocks. Some are also watchdog errors, where the DUT simply stopped responding to commands. In addition to the large-scale SEFIs, there are also cases where only a few bits seem to be affected by an error in the control logic. For example, there are cases where the same two columns will have the same bit in error in consecutive pages. If this pattern holds throughout the memory, it is counted as a SEFI, because there are millions of errors, but that does not seem reasonable, if only a single-digit number of bits are affected. In that case, we have generally counted them as transient bit errors—individual bits that are read incorrectly, but after the exposure, the cell turns out to not be corrupted.

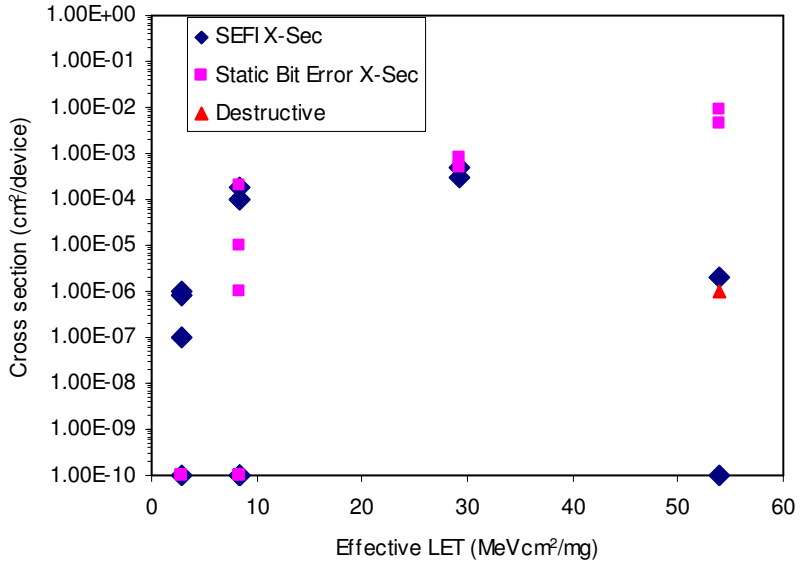

Fig. 5. Results for static mode, with bias applied.

The results for static mode with bias applied are shown in Fig. 5. The SEFI cross section is equal or greater than the bit error cross section at all but the highest LET. These SEFIs are mostly block errors, where every bit in a 128Kx8 block is read as a zero (compared to a checkerboard that was actually stored). After the beam is turned off, multiple reads produce the same result, until power is cycled. After cycling power, the DUT can be read normally—the stored pattern is still stored, except for perhaps the occasional single bit error. Thus, there is a relatively simple way to recover from SEFIs in these NAND flash chips, because the nonvolatile technology is designed to retain information with the power turned off. The recovery method

described here also works in all the other test modes, although the SEFI rate is initially higher in some of the dynamic test modes. We note that the single bit error cross sections in Fig. 5 are very similar to those in Fig. 4, although the SEFI rate is higher with bias applied. We also note that there are no results in Fig. 5 for angles other than normal incidence, which is not the case in Fig. 4. Otherwise, the difference in SEFI rates would be even greater. The destructive failure was a latchup, even though the test was not done at elevated temperature or voltage. After cycling power, the erase function did not work.

For the Dynamic Read condition, the parts showed exhibited transient read errors in addition to the bit and Block errors, and other SEFIs, which are plotted in Fig. 6. In this mode, the DUT reads continuously with the beam on. The SEFI cross sections in Fig. 6 are roughly two orders of magnitude larger than the static mode results in Fig. 5. This result is not surprising—the more functions the control logic performs with the beam on, the more likely it is to have major errors. The static bit errors are those remaining after power is cycled, as before, and also as they will be for the remaining test modes. Transient bit errors, again, will be those that reset when power is cycled, if not before. Some transient errors are bits read erroneously, due to noise in the read circuit, which will be read correctly on the next pass through the memory. Others will be repeated on subsequent reads, but they are corrected by cycling power.

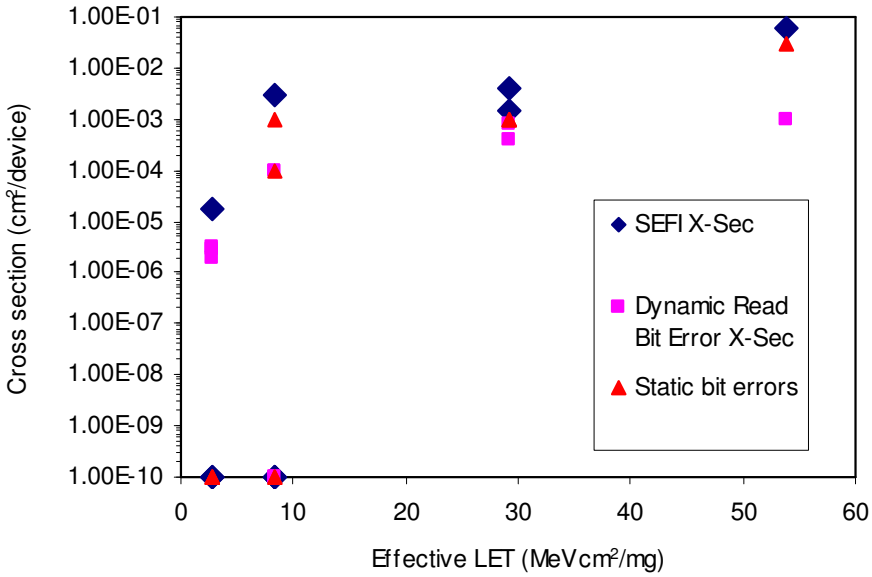

Fig. 6. Results for Dynamic Read mode.

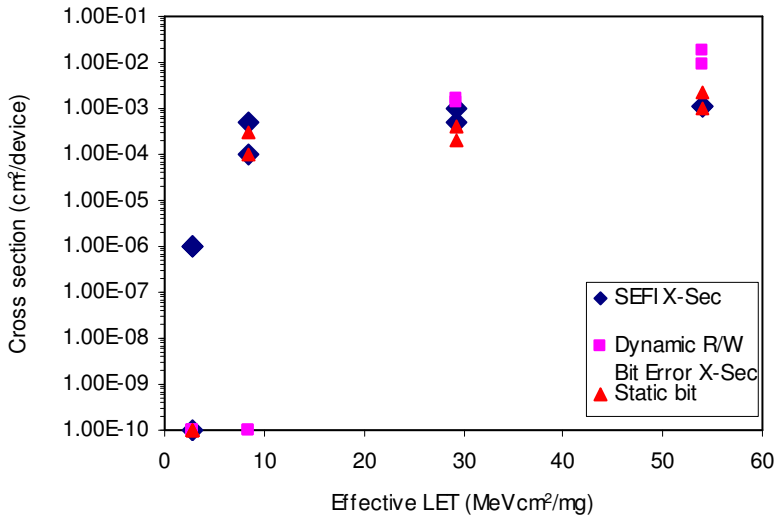

Fig. 7. Results for Dynamic Read/Wright mode.

Results of the dynamic R/W tests are shown in Fig. 7. Generally these results are unremarkable, because the usual zero-to-one errors are rewritten as they occur. For this reason, there are fewer errors indicated than in Fig. 6, although the difference is not large. The main reason for including this test was the expectation that the high voltage write operation would contribute to more errors in the control circuits, but this appears not to have happened, at least not on a large scale. Probably, this is because the write operation is performed only when a zero-to-one error is detected. For this circuit, there are relatively few such errors, so the write circuit duty cycle is a very small number. Where a static cross section is given, it is based on the number of errors detected after the exposure and resetting of the DUT, as before. The transient cross section is based on errors detected during the exposure. But some of the transient errors are probably really static bit errors that were rewritten during the test.

Results for the dynamic R/E/W tests are shown in Fig. 8, to the extent that they can be determined. For this condition, there were many more SEFIs than in the R/W (without erase) mode, which is probably due to the fact that every block is erased and rewritten on every cycle, so that the duty cycle for high voltage operations is much higher. As a practical matter, there are many page and block errors, which usually appear to be independent, on almost every shot with LET at or above 8.4 (Ar). With many large chunks of the memory completely knocked out, it becomes difficult to determine static or transient errors affecting only single bits. The one destructive failure was a latchup, with current jumping to about 80 mA almost as soon as the beam was turned on and staying there until power was cycled, about two minutes later. Afterwards, the DUT could be read normally, but the erase function had been destroyed. This exposure was performed at T=70º C, and V_{dd}=3.6 V.

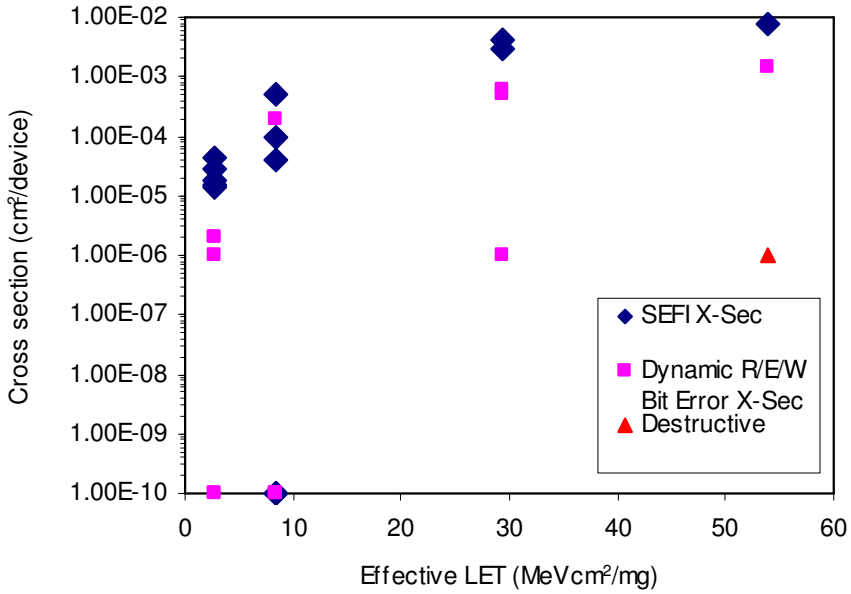

Fig. 8. Dynamic Read/Erase/Write results.

VII. Recommendations

These parts had been tested previously for total dose (TID) response, with all parts functional to 200 krads (SiO_2). Flash memories normally have a few bad blocks, which are identified and screened out. The manufacturer's specification for these parts is 80 or fewer bad blocks, although ten is more nearly typical, in our experience. The only degradation we observed from TID was that some of the parts had one or a few extra blocks go bad, between 100 and 200 krads (SiO_2). In these cases, one might have to screen out 12 bad blocks, compared to ten pre-irradiation. Otherwise, they were all still fully functional, at a dose far above the system requirement.

The SEU response (single bit upset rate) of all NAND flash parts is excellent, compared with standard volatile memories, especially if error correction is used. The SEFI (Single Event Functional Interrupt) rate is of greater concern for space applications than the bit error rate, however. Typically, a SEFI occurs when a control circuit malfunctions as a result of a single ion interaction, and the entire memory, or a large part of it, fails. For standard volatile memories, this may mean reloading the entire memory from a backup, or even rebooting the entire system. For the nonvolatile NAND flash tested here, it is sufficient to cycle power to the system, or at least to the affected part of the system. The SEFI rate here, and in our previous Micron tests, is far above that for other flash memory. At the LET of Ar, the SEFI cross section is typically 10^{-3} or 10^{-4} cm^2/device, which means a SEFI for every 10^3-10^4 incident particles. If we take the geometric mean as a typical number, then we can assume a SEFI every 3000 incident particles with LET =8 or higher. According to the Creme96 input spectrum for geosynchronous orbit, the omnidirectional flux at LET=8 or higher is about 600 particles/cm^2-year. That is, a single chip would be expected to have a SEFI about every five years. A solid state recorder with 600 or 700 chips would have one about every three days. In our previous testing, other manufacturers have done significantly better. The destructive failures from latchup, and also from non-normal

incident particles are potentially serious problems. Latchup only happened at LET = 54, where the flux in geosynchronous orbit is about one particle/cm^2 per 125 years, so the rate might be expected to be low. But the destructive failure at 45º occurred at LET=8.4. The cross section given in Fig 4 is small, because the fluence for the exposure was 10^7 particles/cm^2. But as we have already pointed out, the DUT was not actively monitored during the static shot—the failure could have happened early in the exposure, when the fluence was much lower. It is imperative to better quantify the angular response of these parts before they are used in space—in space, the flux is omnidirectional.

VIII. Further Test Requirements

If these Micron NAND flash memories are to be used in space, it is critical to characterize the angular response. Although there is only a small amount of data at angles other than normal incidence, there was a destructive failure where one would not normally be expected. Quantifying the destructive failure rate is something that absolutely has to be done.

Static Unbiased Test Mode

Shot	Ion/LET	Fluence	Block Errors	Other SEFI	Transient Bit Errors	Static Bit Errors	Comments
26	Ne/2.8	1.00E+06	0	0	N/A	0	
27	Ne/2.8	1.00E+07	0	0	N/A	0	
28	Ne/2.8	1.00E+07	0	0	N/A	0	
39	Ne/2.8	1.00E+06	0	0	N/A	0	
9	Ar/8.4	1.00E+04	0	0	N/A	0	
10	Ar/8.4	1.00E+06	0	0	N/A	1	
11	Ar/8.4	1.00E+07	0	0	N/A	26	
12	Ar/8.4	1.00E+07	0	0	N/A	22	
13	Ar/8.4	1.00E+07	0	1	N/A	3	45 degree incidence; 3M bits
14	Ar/8.4	1.00E+07	1	0	N/A	3	45degree incidence; destructive failure
54	Kr	1.00E+04	0	0	N/A	13	
55	Kr	1.00E+04	0	0	N/A	10	
46	Xe	1.00E+06	0	1	N/A	8400	

Ion	Fluence	Total Bits	Total SEFI	Bit X-sec (cm2/bit)	SEFI X-sec (cm2/device)	Comments
Ne	2.20E+07	0	0	0	0	
Ar	2.10E+07	49	0	5.80E-16	0	normal inc. only
Kr	2.00E+04	23	0	2.90E-13	0	
Xe	1.00E+06	8400	1	2.10E-12	1.00E-06	

Static Mode with Bias

Shot	Ion/LET	Fluence	Block Errors	Other SEFI	Transient Bit Errors	Static Bit Errors	Comments
29	Ne/2.8	1.00E+07	8	0	N/A	0	
30	Ne/2.8	1.00E+07	0	1	N/A	0	
40	Ne/2.8	1.00E+06	0	0	N/A	0	
41	Ne/2.8	1.00E+06	1	0	N/A	0	
1	Ar/8.4	1.00E+06	0	0	N/A	1	
2	Ar/8.4	1.00E+05	17	1	N/A	1	
3	Ar/8.4	1.00E+04	0	1	N/A	2	
4	Ar/8.4	1.00E+03	0	0	N/A	0	
5	Ar/8.4	1.00E+03	0	0	N/A	0	
6	Ar/8.4	1.00E+04	1	0	N/A	0	
7	Ar/8.4	1.00E+03	0	0	N/A	0	
8	Ar/8.4	1.00E+03	0	0	N/A	0	
56	Kr/29.3	1.00E+04	3	0	N/A	8	
57	Kr/29.3	1.00E+04	5	0	N/A	5	
47	Xe/53.9	1.00E+06	0	0	N/A	8657	
48	Xe/53.9	1.00E+06	1	1	N/A	appr. 4500	destr. Latch, no erase

Ion	Fluence	Total Bits	Total SEFI	Bit X-sec (cm2/bit)	SEFI X-sec (cm2/device)	Comments
Ne	2.20E+07	0	10	0	4.50E-07	
Ar	1.12E+06	4	20	8.00E-16	1.77E-05	
Kr	2.00E+04	13	8	2.90E-13	4.00E-04	
Xe	2.00E+06	13150	2	2.18E-12	1.00E-06	

Dynamic Read Mode

Shot	Ion/LET	Fluence	Block Errors	Other SEFI	Transient Bit Errors	Static Bit Errors	Comments
31	Ne/2.8	2.90E+06	8	1	??	0	
31	Ne/2.8	1.00E+06	1	1	??	0	
42	Ne/2.8	1.00E+06	3	0	18	0	
15	Ar/8.4	1.00E+04	1	0	3	0	
16	Ar/8.4	1.00E+03	0	0	0	0	
17	Ar/8.4	1.00E+03	0	0	0	1	
18	Ar/8.4	1.00E+04	1	0	0	1	
58	Kr/29.3	1.00E+04	4	0	40+	10	
59	Kr/29.3	1.00E+04	8	0	14	10	
52	Xe/53.9	1.00E+04	10	0	601	292	

Ion	Fluence	Total bits	Total SEFI	Bit X-sec (cm2/bit)	SEFI X-sec (cm2/device)
Ne	4.90E+06	0	14	0	2.90E-06
Ar	2.20E+04	2	2	2.25E-14	9.10E-05
Kr	2.00E+04	20	12	2.50E-13	6.00E-04
Xe	1.00E+04	292	10	7.30E-12	1.00E-03

Dynamic Read/Write Mode

Shot	Ion/LET	Fluence	Block Errors	Other SEFI	Transient Bit Errors	Static Bit Errors	Comments
33	Ne/2.8	1.00E+06	1	0	??	0	
34	Ne/2.8	1.00E+06	0	0	??	0	
35	Ne/2.8	1.00E+06	0	1	??	0	
43	Ne/2.8	1.00E+06	1	0	??	0	
19	Ar/8.4	1.00E+04	5	0	??	1	
25	Ar/8.4	1.00E+04	1	0	??	3	
60	Kr/29.3	1.00E+04	5	0	17	2	
61	Kr/29.3	1.00E+04	10	0	14	4	
50	Xe/53.9	1.25E+04	14	0	117	28	
51	Xe/53.9	1.00E+04	11	0	188	10	

Ion	Fluence	Total bits	Total SEFI	Bit X-sec (cm2/bit)	SEFI X-sec (cm2/device)
Ne	4.00E+06	0	3	0	7.50E-07
Ar	2.00E+04	4	6	5.00E-14	3.00E-04
Kr	2.00E+04	6	15	7.50E-14	7.50E-04
Xe	2.25E+04	38	25	4.23E-13	1.10E-03

Dynamic Read/Erase/Write Mode

Shot	Ion/LET	Fluence	Block Errors	Other SEFI	Transient Bit Errors	Static Bit Errors	Comments
36	Ne/2.8	1.00E+06	1	0	14	0	
37	Ne/2.8	1.00E+06	0	0	45	0	
38	Ne/2.8	1.00E+06	0	0	27	0	
44	Ne/2.8	1.00E+06	2	0	15	0	
45	Ne/2.8	1.00E+06	2	0	18	0	
20	Ar/8.4	1.00E+04	2	0	5	0	
21	Ar/8.4	1.00E+04	0	0	1	0	
22	Ar/8.4	1.00E+03	0	0	0	0	
23	Ar/8.4	1.00E+04	0	0	0	0	
24	Ar/8.4	1.00E+05	0	0	4	0	
62	Kr/29.3	1.00E+04	6	0	40	0	
63	Kr/29.3	1.00E+04	5	0	30	0	
64	Kr/29.3	1.00E+06	??	1	??	??	Every block affected--many errors
49	Xe/53.9	1.00E+06					Latchup--destructive, no erase
53	Xe/53.9	1.00E+04	15	0	77	3	

Totals	Ion	Fluence	Total bits	Total SEFI	Bit X-sec (cm2/bit)	SEFI X-sec (cm2/device)	Comments
	Ne	5.00E+06	0	5	0	1.00E-06	
	Ar	1.31E+05	0	2	0.00E+00	1.53E-05	
	Kr	1.02E+06	0	12	0.00E+00	5.50E-04	
	Xe	1.01E+06	3	15	7.50E-14	1.50E-03	